

4.2V-60V Vin, 1A, High Efficiency Step-down DCDC Converter with Programmable Frequency

FEATURES

- Wide Input Range: 4.2V-60V
- 1A Continuous Output Current
- $0.8V \pm 1\%$ Feedback Reference Voltage
- Integrated 220mΩ High-Side MOSFET
- Low Quiescent Current: 100uA
- Pulse Skipping Mode (PSM) in light load
- 100ns Minimum On-time
- 4ms Internal Soft-start Time
- Internal compensation for Ease of Use
- Adjustable Frequency 100KHz to 1.2MHz
- External Clock Synchronization
- UV and OV Power Good Output
- Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Low Dropout Mode Operation
- Over-voltage and Over-Temperature Protection
- Available in an ESOP-8L Package

APPLICATIONS

- 12-V, 24-V, 48-V Industry and Telecom Power System
- Industrial Automation and Motor Control
- Vehicle Accessories

DESCRIPTION

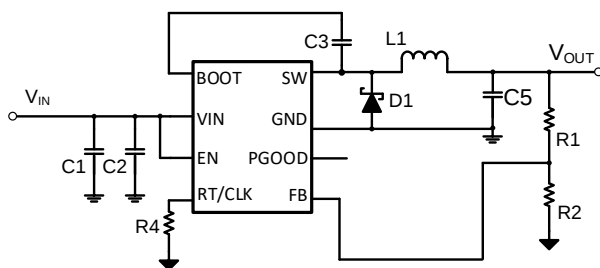
The SCT2612 is 1A buck converter with wide input voltage, ranging from 4.2V to 60V, which integrates an 220mΩ high-side MOSFET. The SCT2612, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) which assists the converter on achieving high efficiency at light load or standby condition.

The SCT2612 features programmable switching frequency from 100 kHz to 1.2 MHz with an external resistor, which provides the flexibility to optimize either efficiency or external component size. The converter supports external clock synchronization with a frequency band from 100kHz to 1.2MHz. The SCT2612 allows power conversion from high input voltage to low output voltage with a minimum 100ns on-time of high-side MOSFET.

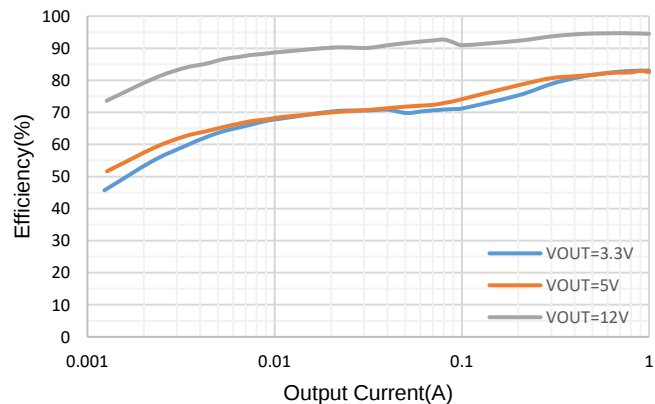
The device offers fixed 4ms soft start to prevent inrush current during the startup of output voltage ramping. The SCT2612 features internal loop compensation to simplify the loop compensation design.

The SCT2612 provides cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in an 8-pin ESOP-8 package.

TYPICAL APPLICATION



4.2V-60V, Asynchronous Buck Converter



Efficiency, Vin=24V, Fsw=500KHz

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production.

Revision 1.1: Update DEVICE ORDER INFORMATION and Input voltage range.

Revision 1.2: Update THERMAL INFORMATION and Figure 24.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT2612STER	Tape & Reel	4000	2612	8	ESOP-8L

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted⁽¹⁾

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	65	V
BOOT	-0.3	72	V
SW	-1	65	V
BOOT-SW	-0.3	6	V
PGOOD, FB, RT/CLK	-0.3	6	V
Operating junction temperature T _J ⁽²⁾	-40	150	°C
Storage temperature T _{STG}	-65	150	°C

PIN CONFIGURATION

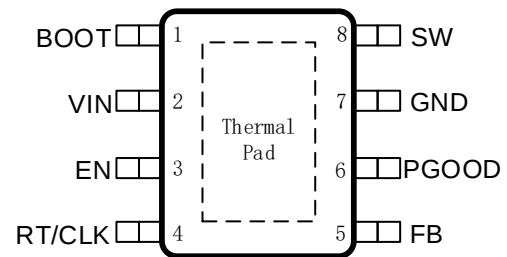


Figure 1. 8-Lead Plastic ESOP

- (1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
- (2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
BOOT	1	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when SW voltage is low.
VIN	2	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
EN	3	Enable pin to the regulator with internal pull-up current source. Pull below 1.05V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
RT/CLK	4	Set the internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to the RT/CLK pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the operation mode automatically returns to resistor programmed frequency.
FB	5	Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 0.8V typical.

PGOOD	6	An open drain output, asserts low if output voltage is low due to thermal shutdown, dropout, over-voltage or EN shut down.
GND	7	Ground
SW	8	Regulator switching output. Connect SW to an external power inductor
Thermal Pad	9	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V _{IN}	Input voltage range	4.2	60	V
V _{OUT}	Output voltage range	0.8	57	V
T _J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V _{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins ⁽¹⁾	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins ⁽²⁾	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	ESOP-8L	UNIT
R _{θJA} ⁽¹⁾⁽²⁾	Junction to ambient thermal resistance	37.39	°C/W
Ψ _{JT} ⁽²⁾	Junction-to-top characterization parameter	7.16	
Ψ _{JB} ⁽²⁾	Junction-to-board characterization parameter	16.44	
R _{θJc} top ⁽¹⁾⁽²⁾	Junction to case thermal resistance	71.77	
R _{θJB} ⁽²⁾	Junction-to-board thermal resistance	16.92	

(1) SCT provides R_{θJA} and R_{θJC} numbers only as reference to estimate junction temperatures of the devices. R_{θJA} and R_{θJC} are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2612 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2612. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R_{θJA} and R_{θJC}.

(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V _{IN}	Operating input voltage		4.2		60	V

SCT2612

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V _{IN_UVLO}	Input UVLO Threshold Hysteresis	V _{IN} rising		3.5 400		V mV
I _{SHDN}	Shutdown current from VIN pin	EN=0, no load		2	5	μA
I _Q	Quiescent current from VIN pin	EN floating, no load, non-switching, BOOT-SW=5V, R _{RT} =200 kΩ		100		μA

Power MOSFETs

R _{DS(on)_H}	High-side MOSFET on-resistance	V _{BOOT} -V _{SW} =5V		220		mΩ
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Reference

V _{REF}	Reference voltage of FB		0.792	0.8	0.808	V
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Current Limit and Over Current Protection

I _{LIM_HS}	High-side power MOSFET peak current limit threshold		2.4	2.8	3.2	A
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Enable and Soft Startup

V _{EN_H}	Enable high threshold			1.2		V
V _{EN_L}	Enable low threshold			1.05		V
I _{EN_L}	Enable pin pull-up current	EN=1V		1		μA
I _{EN_H}	Enable pin pull-up current	EN=1.5V		4		uA
T _{SS}	Soft start time			4		ms

Switching Frequency and External Clock Synchronization

F _{RANGE_RT}	Frequency range using RT mode		100		1200	kHz
F _{SW}	Switching frequency	R _{RT} =200 kΩ(1%)	450	500	550	kHz
F _{RANGE_CLK}	Frequency range using CLK mode		100		1200	kHz
t _{ON_MIN}	Minimum on-time	V _{IN} =24V		100		ns

Power Good

V _{PG_UV}	Power-good flag under voltage tripping threshold	POWER GOOD (% of FB voltage)		95		%
		POWER BAD (% of FB voltage)		90		%
V _{PG_OV}	Power-good flag over voltage tripping threshold	POWER BAD (% of FB voltage)		110		%
		POWER GOOD (% of FB voltage)		105		%
I _{PG}	PGOOD leakage current at high level output	V _{Pull-Up} = 5V			200	nA
V _{PG_LOW}	PGOOD low level output voltage	I _{Pull-Up} = 1 mA		0.1		V

Protection

V _{OVP}	Feedback overvoltage with respect to reference voltage	V _{FB} /V _{REF} rising		110		%
		V _{FB} /V _{REF} falling		105		%
V _{BOOTUV}	reference voltage	BOOT-SW falling		2.5		V
		Hysteresis		230		mV
T _{SD}	Thermal shutdown threshold*	T _J rising		172		°C
		Hysteresis		12		°C

*Derived from bench characterization

TYPICAL CHARACTERISTICS

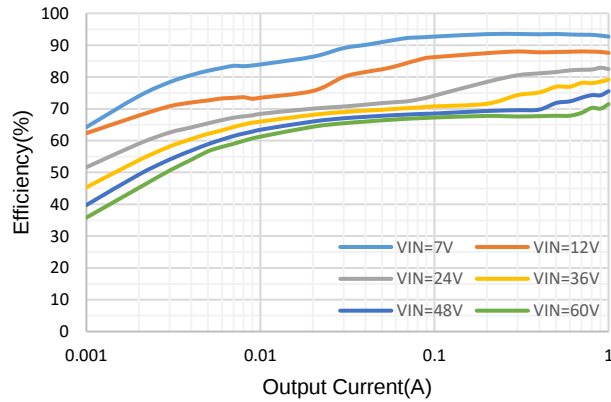


Figure 2. Efficiency vs Load Current, Vout=5V

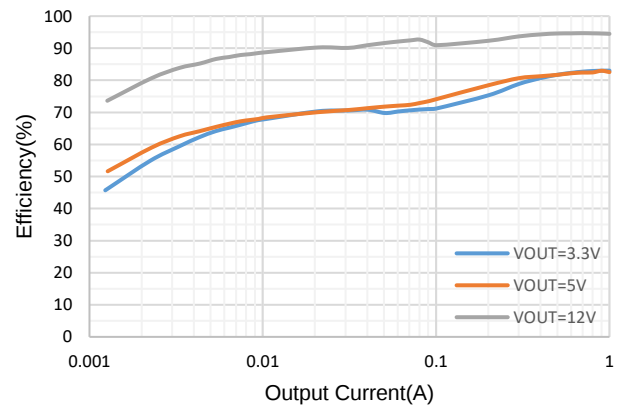


Figure 3. Efficiency vs Load Current, Vin=24V

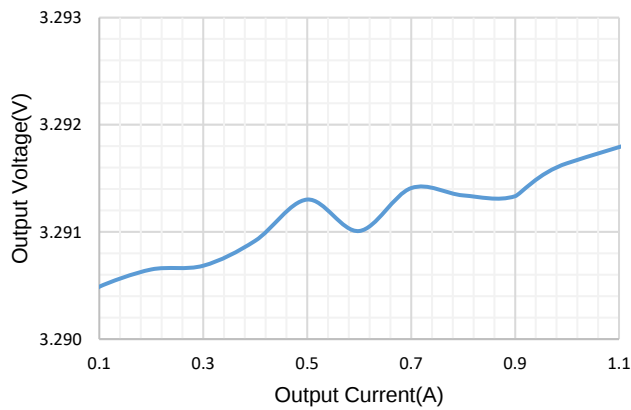


Figure 4. Load Regulation, Vin=24V, Vout=3.3V

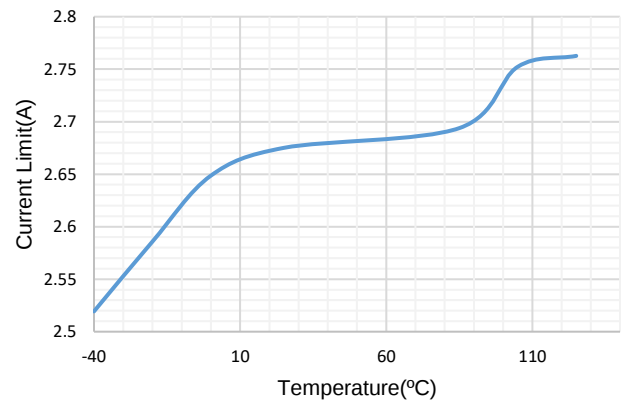


Figure 5. Current Limit VS Temperature

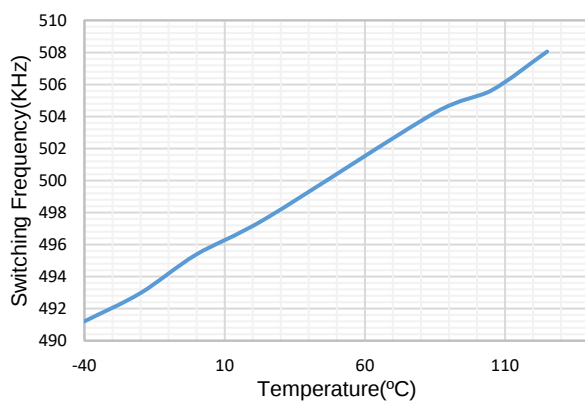


Figure 6. Switching Frequency VS Temperature

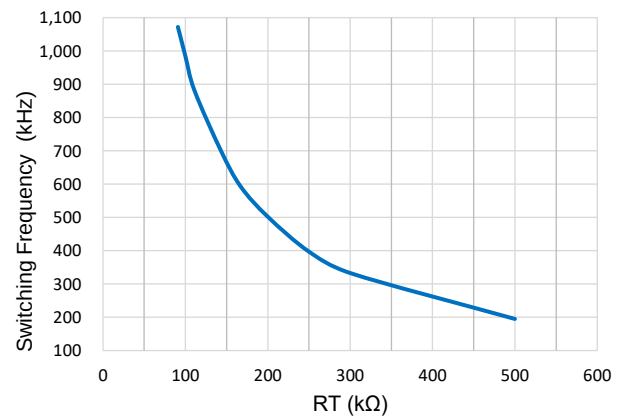


Figure 7. Switching Frequency vs RT Resistor

FUNCTIONAL BLOCK DIAGRAM

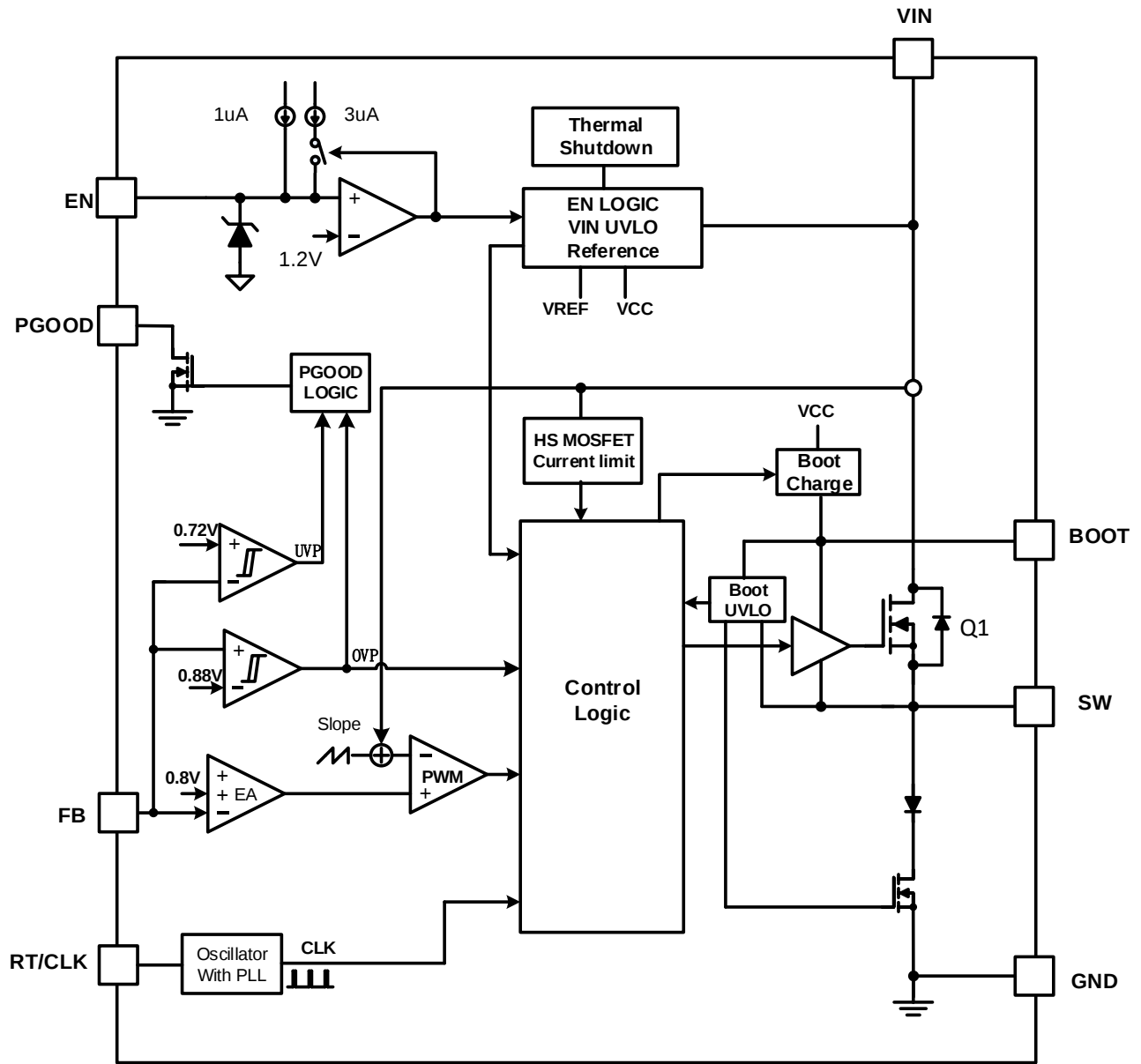


Figure 8. Functional Block Diagram

OPERATION

Overview

The SCT2612 is a 4.2V-60V input, 1A output, buck converter with integrated 220mΩ $R_{ds(on)}$ high-side power MOSFET. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response.

The switching frequency is programmable from 100kHz to 1.2MHz with two setting modes, resistor setting frequency mode and the clock synchronization mode, to optimize either the power efficiency or the external components' sizes. The SCT2612 features internal soft-start to avoid large inrush current. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 100uA under no load or sleep mode condition to achieve high efficiency at light load.

The SCT2612 has a default input start-up voltage of 3.5V with 400mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2612 full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting, output hard short protection and thermal shutdown protection.

Peak Current Mode Control

The SCT2612 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the integrated high-side MOSFET is turned off.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2612 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (470mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 200mA peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 100uA during skipping period with no switching to improve efficiency further.

Enable and Under Voltage Lockout Threshold

The SCT2612 is enabled when the VIN pin voltage rises above 3.5V and the EN pin voltage exceeds the enable threshold of 1.2V. The device is disabled when the VIN pin voltage falls below 3.2V or when the EN pin voltage is below 1.05V. An internal 1uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$R1 = \frac{V_{rise} * 0.875 - V_{fall}}{3.125\mu A} \quad (1)$$

$$R2 = \frac{R1 * 1.05}{V_{fall} - 1.05 + R1 * 4\mu A} \quad (2)$$

where

- V_{rise} is rising threshold of V_{in} UVLO
- V_{fall} is falling threshold of V_{in} UVLO

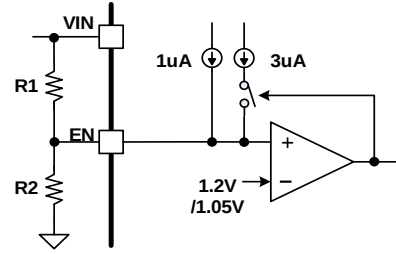


Figure 9. System UVLO by enable divide

Output Voltage

The SCT2612 regulates the internal reference voltage at 0.8V with $\pm 1\%$ tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) * R_{FB_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Switching Frequency and Clock Synchronization

The switching frequency of the SCT2612 is set by placing a resistor between RT/CLK pin and the ground, or synchronizing to an external clock.

In resistor setting frequency mode, a resistor placed between RT/CLK pin to the ground sets the switching frequency over a wide range from 100KHz to 1.2MHz. The RT/CLK pin voltage is typical 0.5V. RT/CLK pin is not allowed to be left floating or shorted to the ground. Use Equation 4 or the plot in Figure 10. to determine the resistance for a switching frequency needed.

$$RT(K\Omega) = \frac{100000}{f_{sw}(KHz)}$$

where, f_{sw} is switching clock frequency

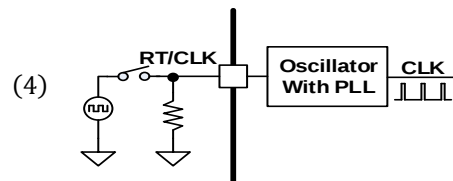


Figure 10. Setting Frequency and Clock Synchronization

In clock synchronization mode, the switching frequency synchronizes to an external clock applied to RT/CLK pin. The synchronization frequency range is from 100KHz to 1.2MHz and the rising edge of the SW synchronizes to the falling edge of the external clock at RT/CLK pin with typical 66ns time delay. A square wave clock signal to RT/CLK pin must have high level no lower than 2V, low level no higher than 0.4V, and pulse width larger than 80ns.

In applications where both resistor setting frequency mode and clock synchronization mode are needed, the device can be configured as shown in Figure 10. Before an external clock is present, the device works in resistor setting frequency mode. When an external clock presents, the device automatically transitions from resistor setting mode to external clock synchronization mode. An internal phase locked loop PLL locks internal clock frequency onto the external clock within typical 85us. The converter transitions from the clock synchronization mode to the resistor setting frequency mode when the external clock disappears.

Bootstrap Voltage Regulator and Low Drop-out Operation

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1 μ F

The UVLO of high-side MOSFET gate driver has rising threshold of 2.5V and hysteresis of 230mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.27V, BOOT UVLO occurs. The converter forces turning on an integrated low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range.

During the condition of ultra-low voltage difference from the input to the output, SCT2612 operates in Low Drop-Out LDO mode. High-side MOSFET remains turning on as long as the BOOT pin to SW pin voltage is higher than BOOT UVLO threshold 2.5V. When the voltage from BOOT to SW drops below 2.27V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Low-side MOSFET only turns on for 100ns in each refresh cycle to minimize the output voltage ripple. Low-side MOSFET may turn on for several times till the bootstrap voltage is charged to higher than 2.5V for high-side MOSFET working normally. The effective duty cycle of the converter during LDO operation can be approaching to 100%.

During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode. As the input voltage is reduced to near the output voltage, i.e. during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO operation mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the SCT2612 LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

Over Current Limit

The SCT2612 implements over current protection with fold back current limit. The SCT2612 cycle-by-cycle limits high-side MOSFET peak current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously.

The SCT2612 implements frequency foldback to protect the converter in unexpected overload or output hard short condition at higher switching frequencies and input voltages. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.8 V to 0 V. The SCT2612 uses a digital frequency foldback to enable synchronization to an external clock during normal start-up and fault conditions. During short-circuit events, the inductor current can exceed the peak current limit because of the high input voltage and the minimum on-time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off-time. The frequency foldback effectively increases the off-time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

With a maximum frequency foldback ratio of 8, there is a maximum frequency at which the inductor current can be controlled by frequency foldback protection. Equation 5 calculates the maximum switching frequency at which the inductor current remains under control when V_{OUT} is forced to V_{OUT_SHORT} . The selected operating frequency must not exceed the calculated value.

$$f_{sw(max skip)} = \frac{f_{DIV}}{t_{min_ON}} \times \left(\frac{I_{LIMIT} \times R_{DC} + V_{OUT_SHORT} + V_d}{V_{IN_MAX} - I_{LIMIT} \times R_{DS(on)} + V_d} \right) \quad (5)$$

where

I_{LIMIT} : Limited average current

R_{DC} : Inductor DC resistance

V_{IN_MAX} : Maximum input voltage

V_{OUT_SHORT} : Output voltage during short

V_d : Diode voltage drop

$R_{DS(on)}$: Integrated high side FET on resistance

T_{min_ON} : Controllable minimum on time

f_{DIV} : Frequency divide equals (1,2,4 or 8)

Over voltage Protection

The SCT2612 implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 0.8V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 0.8V reference voltage, the high-side MOSFET can turn on again.

Power Good (PGOOD)

The PWRGD pin is an open-drain output. A pull up resistor between the values of 10K Ω and 100K Ω to a voltage source that is 5V or less is recommended.

Once the FB pin is between 95% and 105% of the internal voltage reference the PWRGD pin is de-asserted and the pin floats with 260 clock cycles deglitching time. The PWRGD pin is pulled low when the FB is lower than 90% or greater than 110% of the nominal internal reference voltage with 4 clock cycles. Also, the PWRGD is pulled low if Vin UVLO or thermal shutdown are asserted or the EN pin pulled low.

Thermal Shutdown

The SCT2612 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 172 degrees, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 160 degrees, the device restarts with soft start phase.

APPLICATION INFORMATION

Typical Application

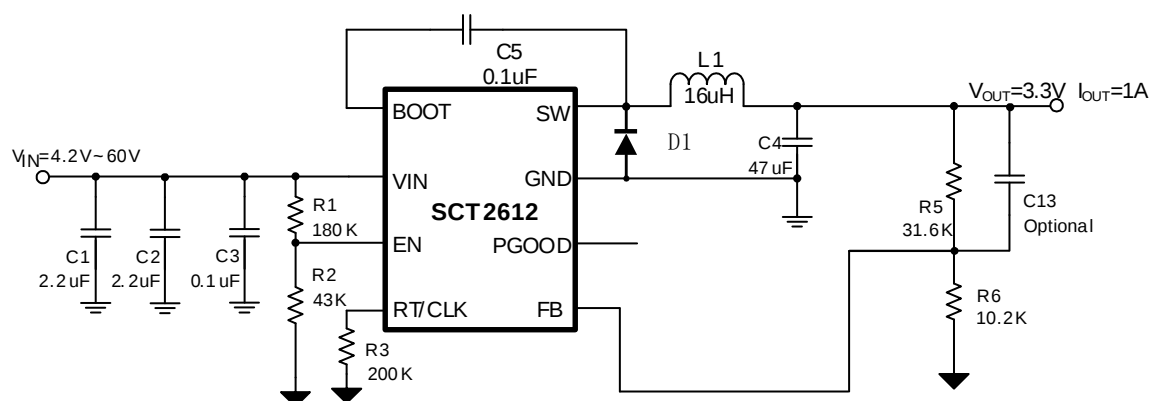


Figure 11. SCT2612 Design Example, 3.3V Output with Programmable UVLO

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 4.2V to 60V
Output Voltage	3.3V
Maximum Output Current	1A
Switching Frequency	500 KHz
Output voltage ripple (peak to peak)	16.5mV
Transient Response 0.25A to 0.75A load step	$\Delta V_{out} = 80\text{mV}$
Start Input Voltage (rising VIN)	5.73V
Stop Input Voltage (falling VIN)	4.045V

Output Voltage

The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 10.2KΩ. Use equation 6 to calculate R5.

$$R_5 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) * R_6 \quad (6)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.8V

Table 1. R5, R6 Value for Common Output Voltage (Room Temperature)

V _{OUT}	R ₅	R ₆
2.5 V	21.5 KΩ	10.2 KΩ
3.3 V	31.6 KΩ	10.2 KΩ
5 V	53.6 KΩ	10.2 KΩ
12 V	143 KΩ	10.2 KΩ
24V	294 KΩ	10.2 KΩ
36V	442 KΩ	10.2 KΩ
48V	604 KΩ	10.2 KΩ

Switching Frequency

Higher switching frequencies support smaller profiles of output inductors and output capacitors, resulting in lower voltage and current ripples. However, the higher switching frequency causes extra switching loss, which downgrades converter's overall power efficiency and thermal performance. The 100ns minimum on-time limitation also restricts the selection of higher switching frequency. In this design, a moderate switching frequency of 500 kHz is selected to achieve both small solution size and high efficiency operation.

The resistor connected from RT/CLK to GND sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using equation 7, or determined from Figure 7.

$$R_3(K\Omega) = \frac{100000}{f_{sw}(KHz)} \quad (7)$$

where:

- f_{sw} is the desired switching frequency

Table 2. R_{FSW} Value for Common Switching Frequencies (Room Temperature)

F _{sw}	R ₃ (R _{FSW})
200 KHz	500 KΩ
330 KHz	301 KΩ
500 KHz	200 KΩ
1100 KHz	90.9 KΩ

Under Voltage Lock-Out

An external voltage divider network of R₁ from the input to EN pin and R₂ from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 5.73V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.045 V (stop or disable). Use Equation 8 and Equation 9 to calculate the values 309 kΩ and 76.8 kΩ of R₁ and R₂ resistors.

$$R_1 = \frac{V_{rise} * 0.875 - V_{fall}}{3.125uA} \quad (8)$$

$$R_2 = \frac{R_1 * 1.05}{V_{fall} - 1.05 + R_1 * 4uA} \quad (9)$$

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 10.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (10)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 11 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (11)$$

Where

- L_{MIN} is the minimum inductance required
- f_{sw} is the switching frequency
- V_{OUT} is the output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 12 and equation 13.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (12)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (13)$$

Where

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 2.8A. The most conservative approach is to choose an inductor with a saturation current rating greater than 2.8A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2612 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Diode Selection

The SCT2612 requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than $V_{IN(max)}$. The peak current rating of the diode must be greater than

the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 60-V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the SCT2612.

For the example design, the B360B-13-F Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the B360B-13-F is 0.7 volts at 3 A.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. At higher switching frequencies, the ac losses of the diode need to be taken into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. Equation 14 is used to calculate the total power dissipation, including conduction losses and ac losses of the diode.

The B360B-13-F diode has a junction capacitance of 200 pF. Using Equation 14, the total loss in the diode at the maximum input voltage is 0.66 W.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{(V_{IN_MAX} - V_{OUT}) \times I_{OUT} \times V_d}{V_{IN_MAX}} + \frac{C_j \times f_{SW} \times (V_{IN} + V_d)^2}{2} \quad (14)$$

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 15.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (15)$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (16)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 17 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (17)$$

For this example, two 2.2μF, X7R ceramic capacitors rated for 100 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 18 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}^2 * L * C_{OUT} * V_{IN}} \quad (18)$$

Where

- ΔV_{OUT} is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, one 47μF ceramic output capacitors work for most applications.

Application Waveforms

Vin=24V, Vout=3.3V, unless otherwise noted

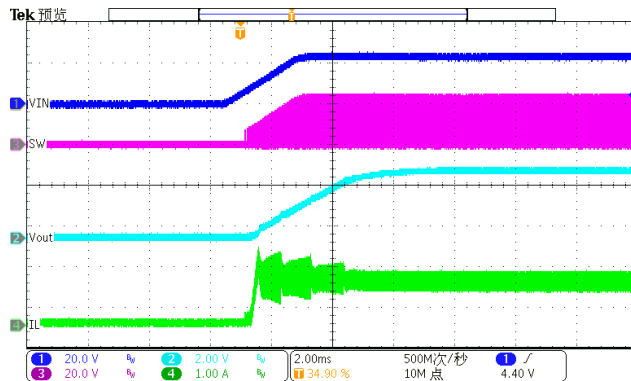


Figure 12. Power up(Iload=1A)

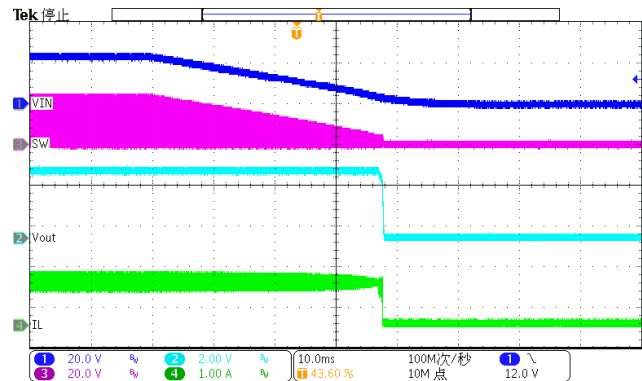


Figure 13. Power down(Iload=1A)

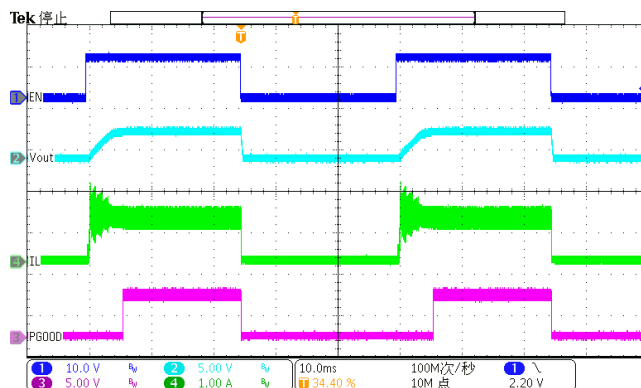


Figure 14. EN toggle (Iload=1A)

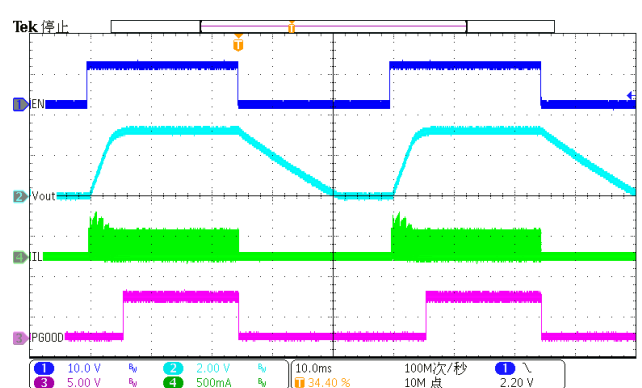


Figure 15. EN toggle (Iload=20mA)

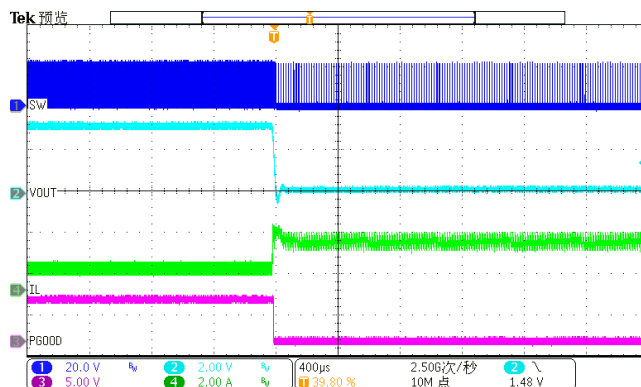


Figure 16. Over Current Protection(1A to hard short)

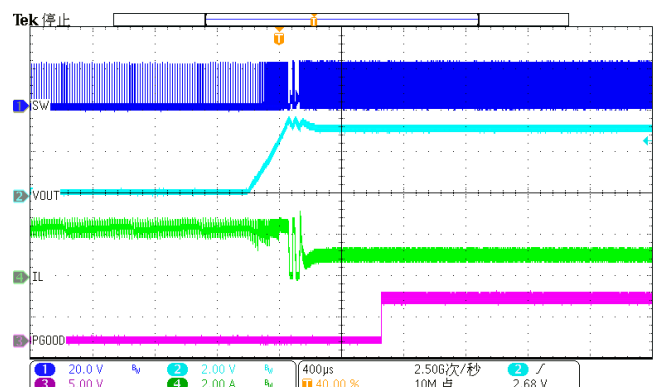


Figure 17. Over Current Release (hard short to 1A)

Application Waveforms(continued)

$V_{in}=24V$, $V_{out}=3.3V$, unless otherwise noted

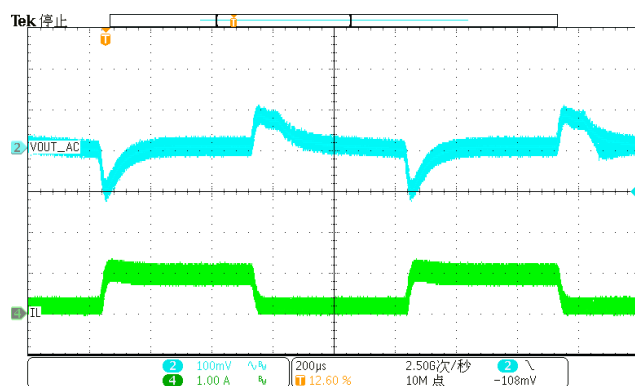


Figure 18. Load Transient (0.1A-0.9A, 1.6A/us)

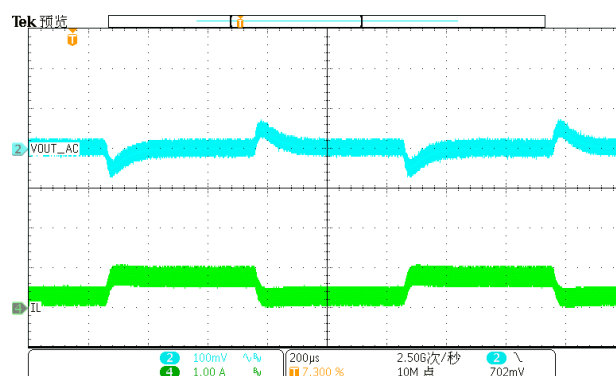


Figure 19. Load Transient (0.25A-0.75A, 1.6A/us)

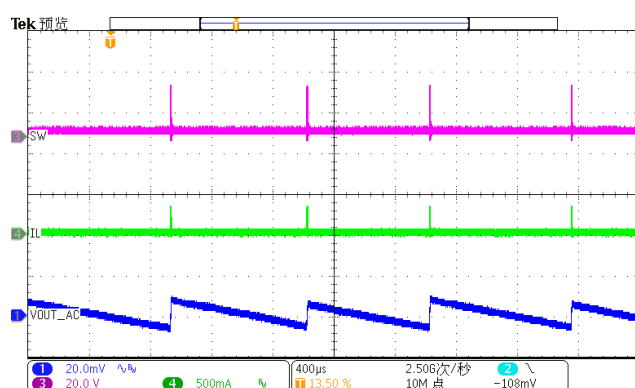


Figure 20. Output Ripple (Iload=0A)

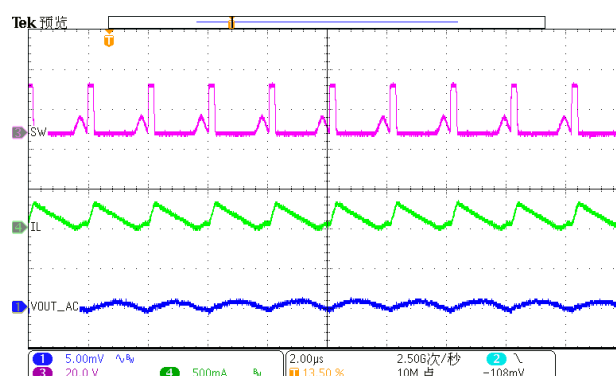


Figure 21. Output Ripple (Iload=100mA)

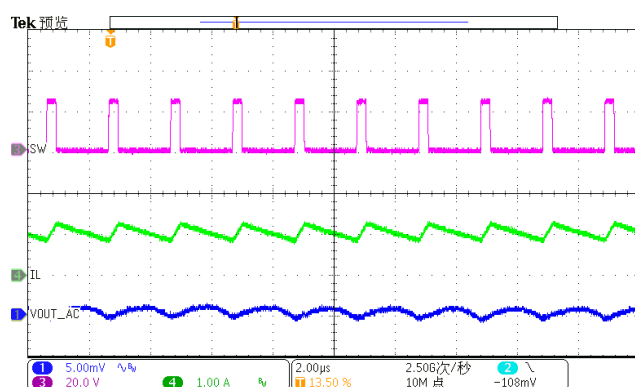


Figure 22. Output Ripple (Iload=1A)

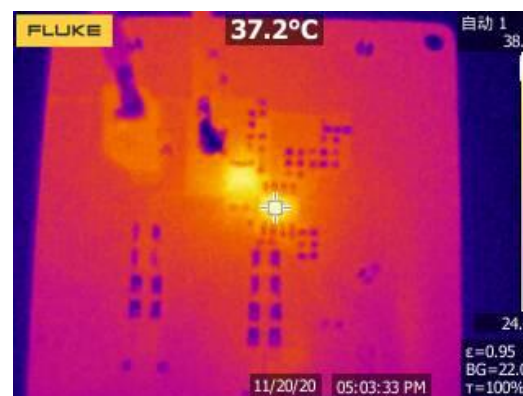


Figure 23. Thermal, 24VIN, 3.3Vout, 1A

Layout Guideline

Proper PCB layout is a critical for SCT2612's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impedance and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. Freewheeling diode should be place as close to SW pin and the ground as possible to reduce parasitic effect.
4. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impedance of grounding.
5. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
6. Output inductor and freewheeling diode should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
7. The RT/CLK terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
8. UVLO adjust, RT resistors and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
9. Route BOOT capacitor trace on the other layer than top layer to provide wide path for topside ground.
10. For achieving better thermal performance, a four-layer layout is strongly recommended.

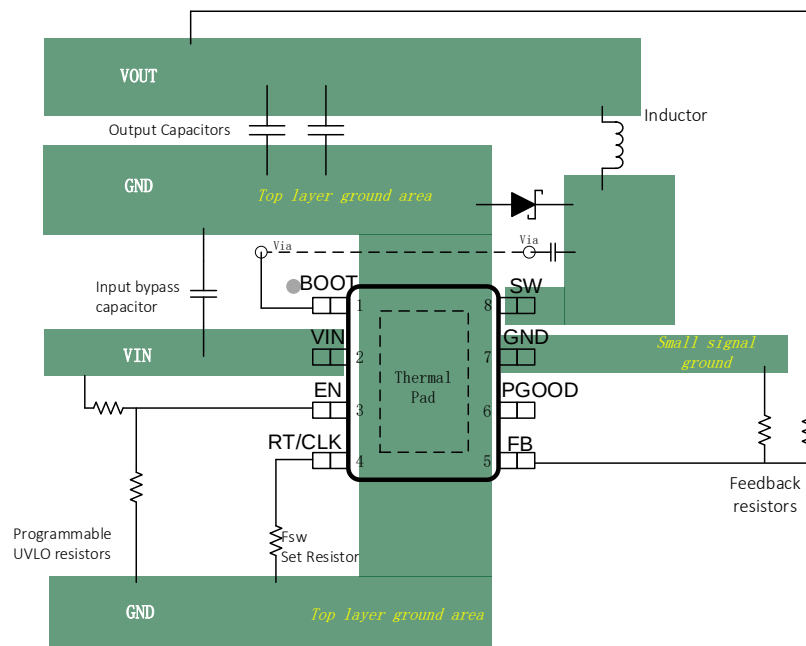
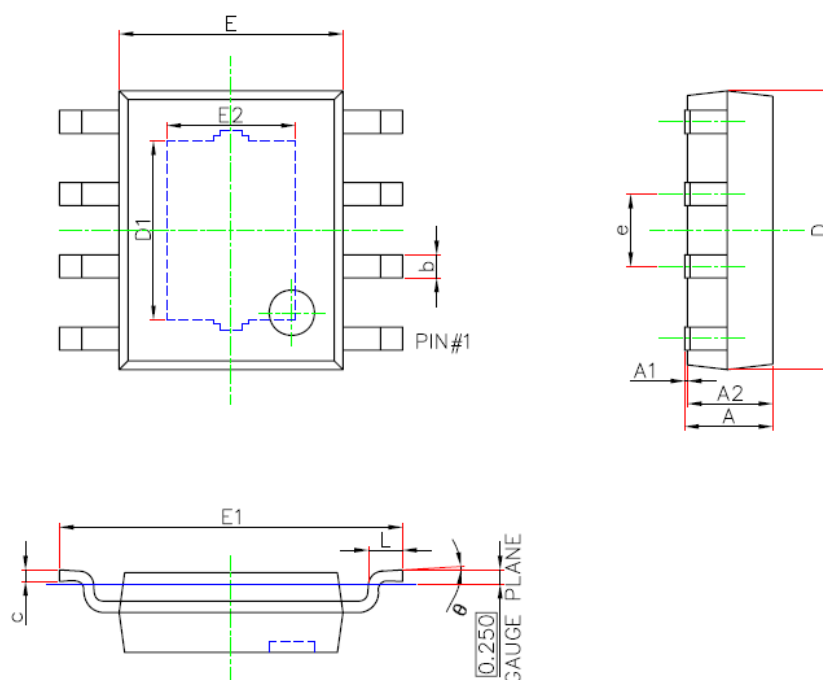


Figure 24. PCB Layout Example

PACKAGE INFORMATION



SOP8/PP(95x130) Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

